Open EDA and Semiconductor Design

Towards an European Roadmap

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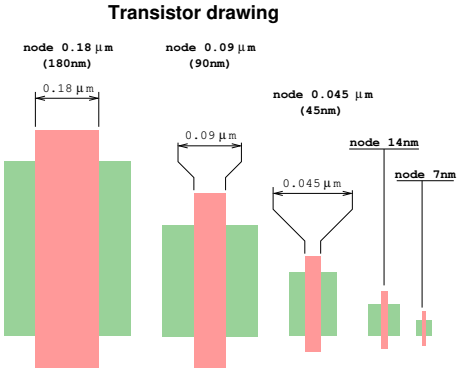
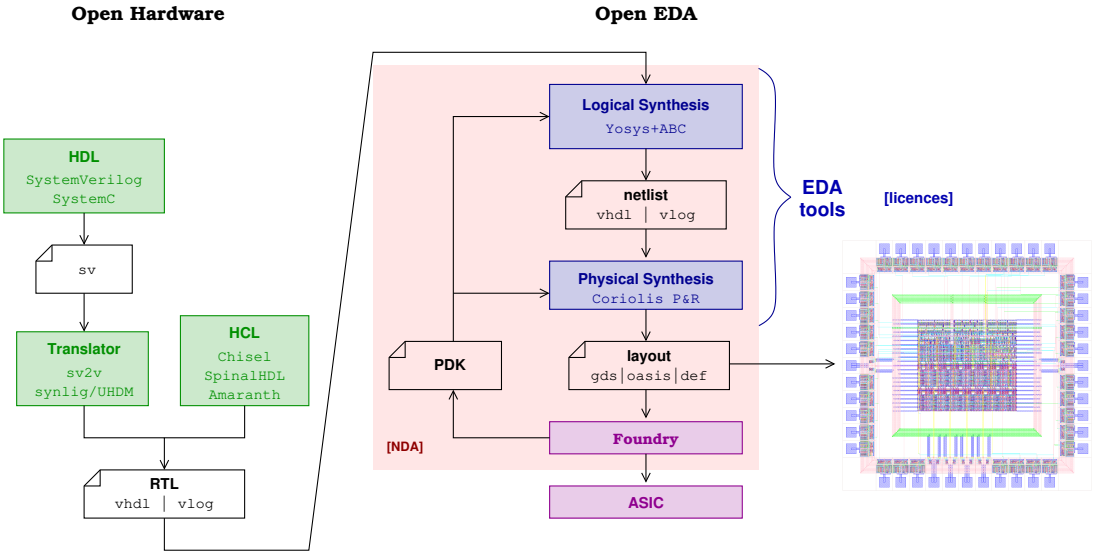
All Flavors of Designs

Type	Status
Digital	Full automation
Analog	Some automation
RF	Simulation tools / hand crafted
MEMS	Simulation tools / hand crafted
Photonics	Simulation tools / hand crafted
Quantum	Simulation tools / hand crafted



Digital Design Flow – Overview



Generative Digital Flow – What we do

Logical synthesis

Physical synthesis

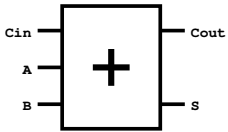
RTL

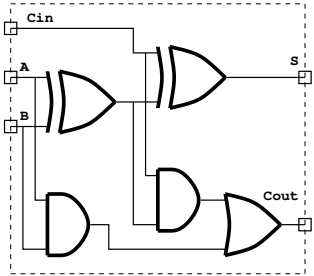
Netlist

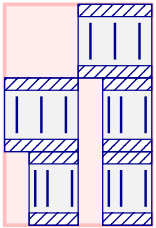
Placement

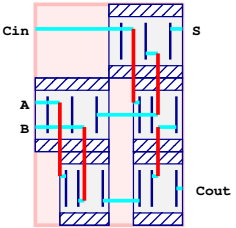
Routing

```
[Cout,S] = A + B + Cin
```

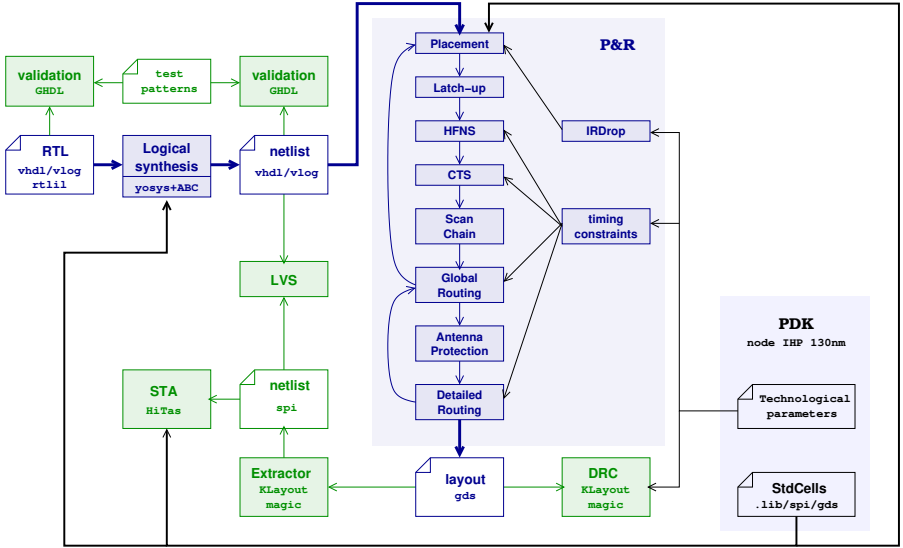






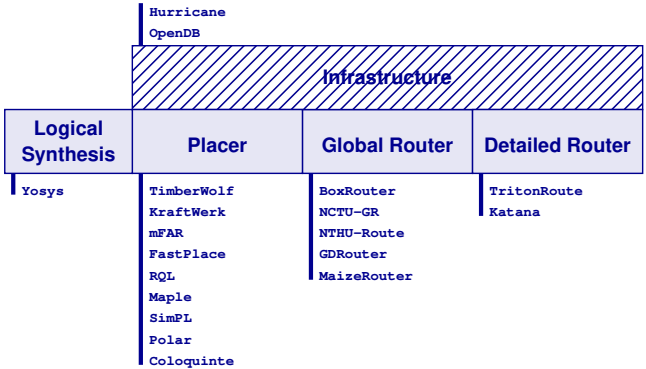


Digital Design Flow – RTL to GDSII

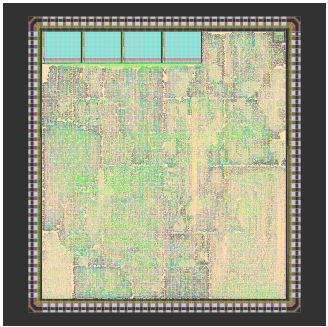


Hardness Metric

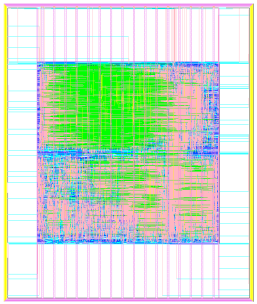
- In order to evaluate the hardness of each step of the toolchain as well as it's implementation complexity, we choose to count the number of published academic softwares.
- Regarding the detailed routing, only two alternatives exists :
  1. `TritonRoute` from OpenROAD.
  2. `Katana` from Coriolis.



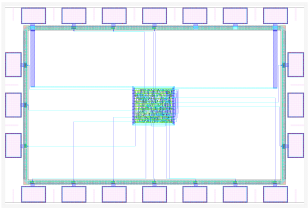
Some Pretty Pictures



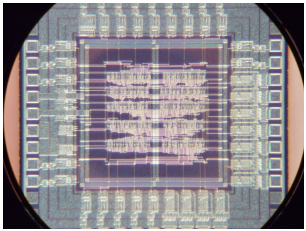
LibreSOC chip, 1.3M transistors
TSMC 0.18µm



Vex RISC-V chip, 220K transistors
SkyWater 0.13µm



Thermometer chip, 1K transistors
Pragmatic 0.8µm (flexible)



Onsemi 1.2µm

Features & Softwares – A Quick Survey

Digital flow		
Feature	**Toolchain**	
	Coriolis	**OpenROAD**
Logical synthesis	**Yosys**	
Placer	✔	✔
Global router	✔	✔
Detailed router	✔	✔
Clock tree (CTS)	H-Tree	balanced
High fanout net synthesis (HFNS)	✔	✔
Latch-up protection	✔	✔
Antenna effect protection	✔	✔
Layer density	partial	partial
IR drop analysis	–	✔
Design rules checking (DRC)	**KLayout /Magic**	
Gate level extraction	✔	OpenRCX
Parasitic extraction	–	
Layout vs. schematic (LVS)	✔	✔
Static timing analysis (STA)	HiTas	OpenSTA
Digital/analog mixed designs (layout)	Native	**FASoC**
Automatic Test Patterns Generation (ATPG)	**Fault Quaigh**	
Multiple clock domains	–	–
Clock gating	–	–
Cell strength scaling	–	–
Scan chain insertion	–	–
Yield optimization	–	–
Thermal analysis	–	–

Open Hardware realm	
SystemVerilog to Verilog	**sv2v** **synlig + surelog** **svase**
Verilog simulator	**Icarus Verilog**
VHDL simulator	**GHDL**
Design test benchs	**cocotb**
Analog Design	
Electrical simulation	**ngspice** **xyce**

Glossary

ASIC Application Specific Integrated Circuit. 3

CTS Clock Tree Synthesis. 5

DRC Design Rule Checking. 5

EDA Electronic Design Automation. 3

HCL Hardware Construction Language. 3

HDL Hardware Description Language. 3

HFNS Hight Fanout Net Synthesis. 5

HLS Hight Level Synthesis. 3

LVS Logical vs. Schematic. 5

PDK Process Design Kit. 5

RTL Register Transfer Logic. 5

STA Static Timing Analysis. 5