Open PDK with Open EDA Tools - Challenges and Future needs

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IHP at a Glance

Positioning

- IHP is the **European research and innovation centre** for **silicon-based systems**, ultrahigh-frequency circuits and technologies

- The research focuses on **socially relevant topics** such as communication, mobility, health & environment, industry & agriculture, sustainability and security.

- **Unique selling point** of a **200mm pilot line** for state-of-the-art BiCMOS technologies, operated under **industry-like conditions, 24/7**, for the provision of prototypes and low-volume production runs.

- **Qualified technological platform** with direct access for science and industry

Vision
"We create foundations and prototype applications based on future silicon-based technologies and systems for a digitalised and networked world as well as for the sustainable preservation of our natural living conditions."

130nm SiGe BiCMOS Technologies for RF Applications

	SG13S	SG13G2	SG13G3Cu
SiGe-HBT f_t/f_{max}	250 / 340 GHz	350 / 450 GHz	**470 / 650 GHz**
$W_{Emitter}$	170 nm	130 nm	110 nm
HBT BV_{CE0}	1.7 V	1.6 V	1.5 V
CMOS node	**130 nm**		
Active devices	Schottky diodes, Antenna diodes, PN diodes, ESD		
Varactors	NMOS Varactor		
Resistors	Poly-Si, Thin Film		Poly-Si
MIM Caps	1.5 fF / µm² (Al) 2.1 fF / µm² (Cu)	1.5 fF / µm² (Al) 2.1 fF / µm² (Cu)	2.1 fF / µm²
Metallization	7 Layers AL incl. 2 & 3 µm layers or *Cu: 4 + 2 (3µm) Al: 2 (3µm)	7 Layers AL incl. 2 & 3 µm layers or *Cu: 4 + 2 (3µm) Al: 2 (3µm	*Cu: 4 + 2 (3µm) Al: 2 (3µm

*Cu BEOL from X FAB

- Target are **high end developments** for RF & Terahertz frequencies, cryo and space applications
- SG13S & SG13G2 are qualified and ready for **Low Volume of high end products SG13G2** technology was selected for the development of an **open PDK**
- SG13G3Cu is early access - qualification scheduled 2025

# Motivation for IHP's open Process Design Kit (PDK) initiative

- **Simplify access to education** materials for chip designers and to attract young people to get into chip design process

- Provide **low threshold (cost/technological) access to technology & PDK** for chip designer, academic projects

- **Be a pioneer** in demonstrating the possibilities of open source EDA software

- To **convince commercial fabs** to support the open source approach

- Support chip design possibilities for **advance IC design projects** by **StartUp, SMEs and commercial companies**

Open EDA cycle to push open hardware development

Enable open and worldwide collaboration on development
of the PDK, co-development of tools and PDK features

Open PDKs

**OPEN SOURCE
EDA DEVELOPMENT
CYCLE**

Open Tools

(Open) Designs
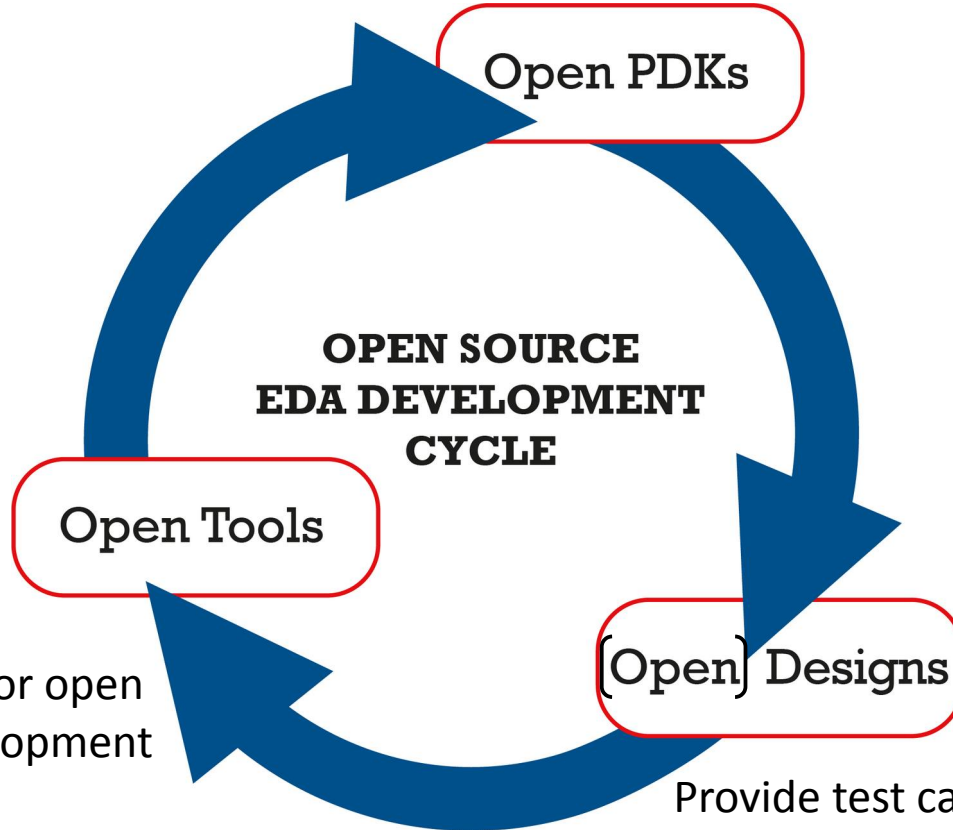
Open EDA Tools for more than 20 years
but
**Open PDK was the missing piece to get
the cycle going**

Provides platform for open
EDA software development
and possibility for
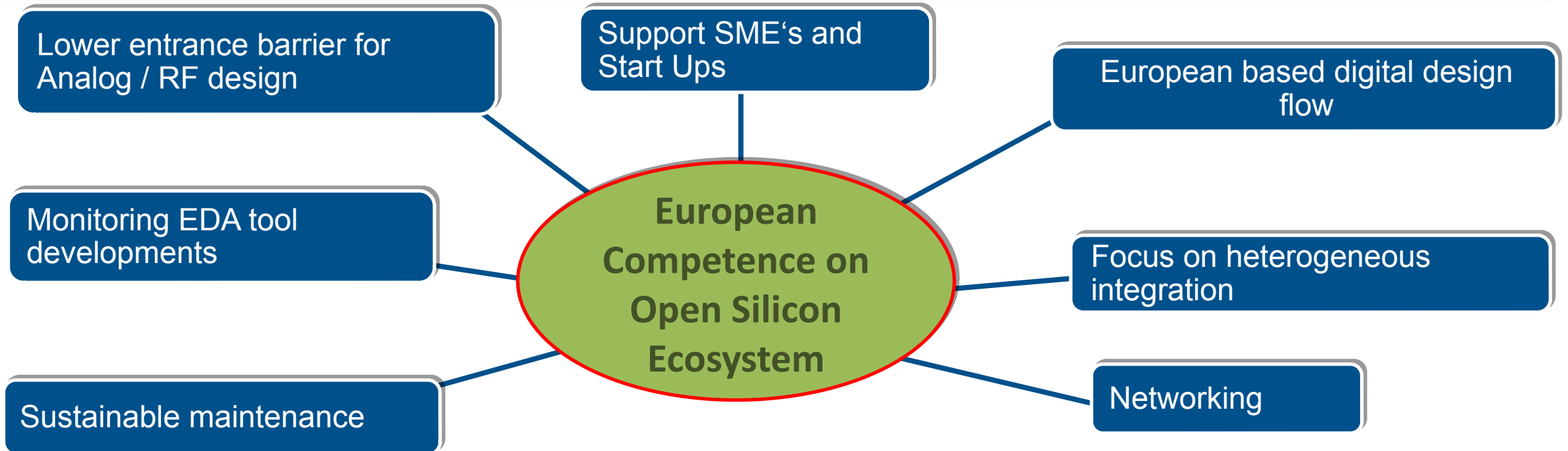collaborative design projects

Provide test cases, regression tests,
benchmarks, use cases, user stories,
feedback & error reports

Analog/RF Open Source Design Flow / Challenges
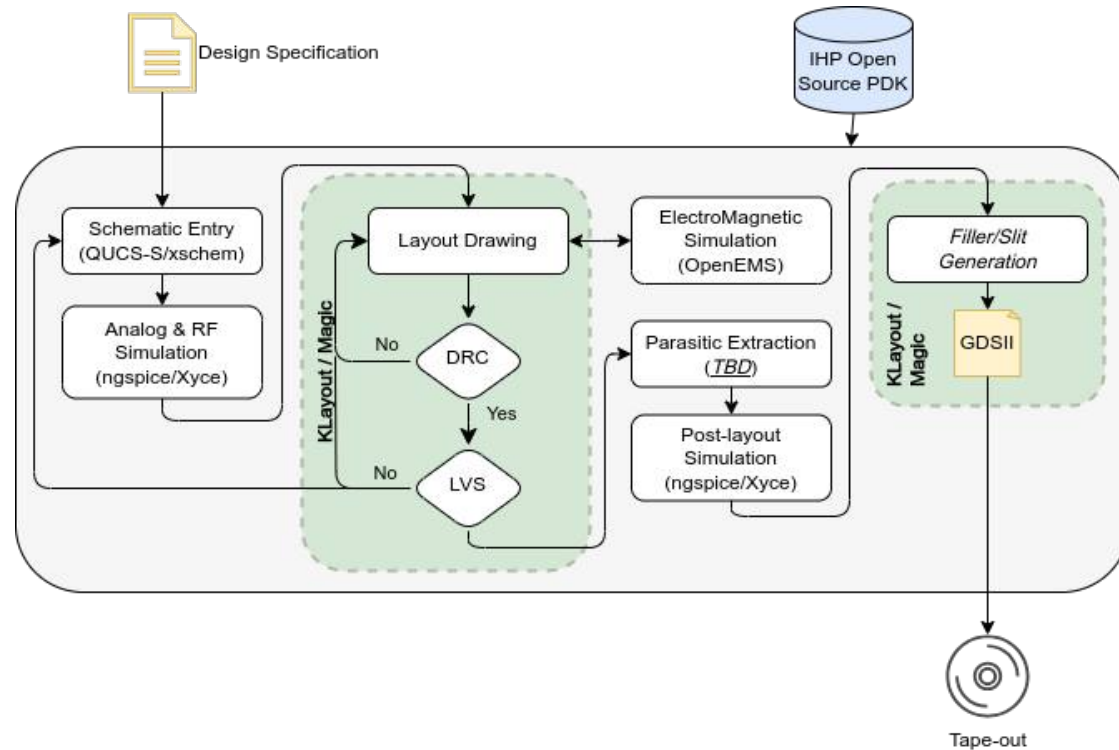
- Open EDA Tools often handled by individual enthusiasts or small groups
- Lack of a complete open source analog design flow
- Open IC designs needed to improve Open EDA tools and foster its developments
- Open Process Design Kits are not available in EU
- No European concept for sustainable maintenance of the Open PDKs and Open EDA tools

Future Needs

Lower entrance barrier for Analog / RF design

Support SME's and Start Ups

European based digital design flow

Monitoring EDA tool developments

European Competence on Open Silicon Ecosystem

Focus on heterogeneous integration

Sustainable maintenance

Networking

- We need a European Open Source Silicon Ecosystem
  - Is a **European Open Silicon Hub** possible?
  - Will there be projects targeting open source to **get initial funding**?
  - Can a **European Foundation** or associated fund support this?

Acknowledgment

- Thanks to open source community SemiMod, ETH Zurich, Uni Linz, ChipFlow, Staf Verhaegen (PDKMaster), M. Koefferlein (klayout), D. Warning, H. Vogt (ngspice), M. Brinson (Qucs-S), and many more …

- Thanks to different public founded German projects:
  - VE-HEP (16KIS1339K)
    https://elektronikforschung.de/projekte/ve-hep-1
  - IHP Open130-G2 (16ME0852)
    https://www.elektronikforschung.de/projekte/ihp-open130-g2
  - FMD-QNC (16ME0831)
    https://www.elektronikforschung.de/projekte/fmd-qnc
  - Design tools for sovereign chip development with open source (DE:Sign) – starting now May 2024

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