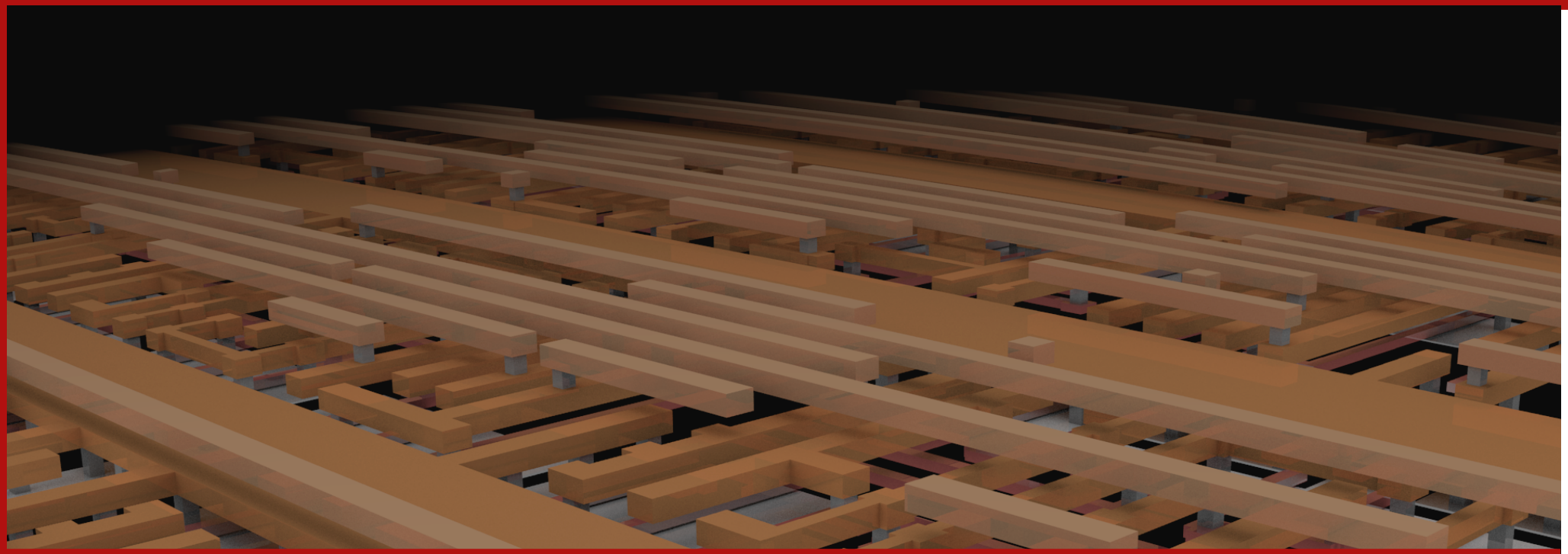

Free and open-source semiconductor ecosystem

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GaT

The challenge

- Most **silicon chips** today are literally **black boxes:**
  - Layout: **practically always secret**
  - High-level design: **very often secret**
  - Some companies use open instruction sets like RISC-V, but their designs remain (most of the times) secret

- Consequences:
  - Limited **security** and limited **trust** (security-by-obscurity vs. security-by-openness)
  - Impossibility to **share** designs

"intel inside"
....but what's inside intel ?!?

Vision

- Enable stakeholders (companies, RTOs, universities, etc) to **open-source** their chip designs *(all the way down to the layout)*
- Enable stakeholders to **share** silicon designs
  - This includes **standard building blocks** (like memories, CPU cores, I/O components, analog blocks, standard-cell libraries)
  - Enable companies to focus on **real** innovation rather than on reinventing the wheel
- Enable companies to develop **new technologies** not supported by mainstream design software (e.g. neuromorphic computers)

Two necessary conditions

- In practice, sharing a silicon chip design **requires** using **open-source Electronic Design Automation (EDA)** tools
  - That's because licence agreements usually don't allow to publish any output generated by mainstream EDA tools
  - Imagine writing a book with Microsoft Word and not being allowed to publish it…
- Publishing a silicon chip design (and its layout in particular) **requires** using a silicon foundry with an **open Process Design Kit (open PDK)**
  - That's because foundries otherwise forbid publishing any of their "secrets"

    → see upcoming talk by IHP Microelectronics

Open-source EDA flow

- OpenROAD (= **R**ealization of **O**pen, **A**ccessible **D**esign)
  - Funded by DARPA until 12/2023 (now a 501(c)(3) non-profit: https://openroadinitiative.org/)
  - Active developers:~30 people at any time (averaged)
  - Budget: ~3M$/year
  - Over 600 tape-outs [1] in GF180nm, SKY130nm, SKY90nm, TSMC 65nm, GF55nm, Intel 22/16nm, GF12LP **(180nm to 12nm)** [1]
  - Tested also by independent groups (e.g. [2] and [3])

[1] OpenROAD: The journey so far and roadmap (Andrew Kahng), https://piped.video/watch?v=z-yoZuJx2IE (2023)
[2] Open-Source and Non-Commercial Software for Digital ASIC Design, I.M. Piatak, O.T. De Laubenque, V.A. Antropov, V.A. Yurchenko, https://ieeexplore.ieee.org/document/10318767 (2023)
[3] Insights from Basilisk: Are Open-Source EDA Tools Ready for a Multi-Million-Gate, Linux-Booting RV64 SoC Design?, P. Sauter, T. Benz, P. Scheffler, F.K. Gürkaynak, L. Benini, https://arxiv.org/pdf/2405.04257 (5/2024)

The Alliance/Coriolis flow

- In Europe: Alliance/Coriolis
- Developed at Sorbonne University since 1990 (see following talk)
- Active developers: 2
- Support for “Symbolic Layout” custom cells [1] to be later translated into foundry’s PDK (tested on AMS 350nm, TSMC 180nm, SkyWater 130nm, one chip each)
- ...more details in the next talk...

[1] Alliance/Coriolis VLSI CAD Tools http://coriolis.lip6.fr/

Silicon libraries: State-of-the-art

- Open-source silicon blocks (**open all the way down to the layout**) are in their infancy

  → one of the first silicon blocks (an ADC) was published by Prof. Harald Pretl et al. in 2023 at FSiC [1]

- RTOs and academics need more incentives for publishing such designs (e.g. seeing such projects recognised for their curricula)
- Enterprises will benefit by a populated library of silicon blocks, but they need also an incentive to contribute to them

  → exploit the advantage of contributing to a widely shared project

  → protect the open-source blocks with suited licences

[1] Design of a 1.2MS/s Charge-Redistribution Non-Binary SAR-ADC Utilizing the SKY130 Open-Source Technology
https://wiki.f-si.org/index.php?title=Design_of_a_1.2MS/s_Charge-Redistribution_Non-Binary_SAR-ADC_Utilizing_the_SKY130_Open-Source_Technology

Funding for open silicon and open EDA

- NLnet [1]
- NGI Zero Commons Fund [2]
- Some funded hardware projects:
  - OpenXC7, kintex-nextpnr, and Apicula (Yosys extensions)
  - SpinalHDL, VexRiscv (popular core)
  - Wishbone-Streaming (bus protocol)
  - ULX3M FPGA development board (available on mouser!)
  - LiteX (framework for building Systems on Chip)
  - MNTReform (lapop as open as it gets)
  - Icestudio (GUI for entry-level FPGA/ASIC design)
  - OpenWifi (FPGA implamentation up to WiFi 6)

[1] https://NLnet.nl/
[2] https://www.ngi.eu/ngi-projects/ngi-zero-commons-fund/

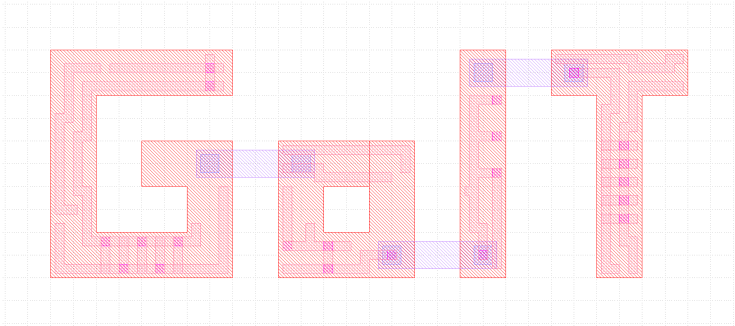
Future needs

- For academia: a **reward mechanism** for open-source development (not just citations, h-factor, etc.)
- For companies: a **“fair-game” licence** for silicon blocks, i.e. a licence which does not allow others to simply *copy-and-disappear* (close the source again)
- We need people who **write** EDA (rare) and people who **use** EDA. People who write EDA must know how to program and should know how to design a chip → **need for new university courses**
- **Sustainability:** A mechanism to foster and **maintain** on the long run EDA software and the silicon libraries (public/private funding entities, coordination entities, standardization activities, etc.)
- … **and many more**…. (see roadmap in [1] and following talks)

[1] Recommendations and roadmap for the development of open-source silicon in the EU
https://wiki.f-si.org/index.php?title=Recommendations_and_roadmap_for_the_development_of_open-source_silicon_in_the_EU

Thank you!

This work is funded by the European Union. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or of the European Commission. Neither the European Union nor the European Commission can be held responsible for them.



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